WHAT IS CLAIMED IS:

1. A method for recycling a charge in a memory device, comprising:

precharging first and second power lines of a first array of bit line sense amplifiers to a first voltage level between an upper reference voltage level and a first intermediate voltage level;

precharging first and second power lines of a second array of bit line sense amplifiers to a second voltage level between a second intermediate voltage level and a lower voltage reference, wherein the second intermediate voltage level is greater than the first intermediate voltage level; and

momentarily coupling the first power line of the second array to the second power line of the first array to transfer charge therefrom.

2. The method of claim 1, further comprising:

decoupling the first power line of the second array from the second power line of the first array;

coupling the second power line of the first array to a first supply line at the first intermediate voltage level; and

coupling the first power line of the second array to a second supply line at the second intermediate voltage level.

3. The method of claim 2, further comprising, prior to decoupling the first power line of the second array from the second power line of the first array:

coupling the first power line of the first array to a supply line at the upper reference voltage level; and

coupling the second power line of the second array to a supply line at the lower reference voltage level.

4. The method of claim 1, wherein the voltage difference between the second intermediate voltage level and the lower reference voltage level is greater than half the voltage difference between the upper reference voltage level and the lower reference voltage level.

5. The method of claim 1, wherein the voltage difference between the upper

reference voltage level and the first intermediate voltage level is greater than half the voltage difference between the upper reference voltage level and the lower reference voltage level.

6. A method for recycling charge comprising:

powering at least a portion of sensing operations of a first array of bit line sense operations with first and second power lines at an upper reference voltage level and a first intermediate voltage level, respectively;

powering at least a portion of sensing operations of a second array of bit line sense operations with first and second power lines at a second intermediate voltage level and a lower reference voltage level, respectively; and

during or prior to the sensing operations, transferring charge from the second power line of the first array to the first power line of the second array.

7. The method of claim 6, wherein transferring charge from the second power line of the first array to the first power line of the second array comprises momentarily closing a first switch to couple the second power line of the first array to the first power line of the second array.

8. The method of claim 7, further comprising:

opening the first switch to decouple the second power line of the first array to the first power line of the second array;

closing at least a second switch to couple the second power line of the first array to a power supply node at the first intermediate voltage level; and

closing at least a third switch to couple the first power line of the second array to a power supply node at the second intermediate voltage level.

9. The method of claim 6, wherein at least one of the first and second intermediate voltage levels is greater than one half the upper reference voltage level when measured from the lower reference voltage level.

10. A method for recycling charge from one or more power lines of a first array of bit line sense amplifiers to one or more power lines of a second array of bit line sense amplifiers, comprising:

momentarily closing a first one or more switches to precharge first and second power lines of the first array to a first voltage level between a first intermediate voltage level and an upper reference voltage level and to precharge first and second power lines of the second array to a second voltage level between a lower reference voltage level and a second intermediate voltage level;

momentarily closing a second one or more switches to transfer charge from the second power line of the first array to the first power line of the second array; and

momentarily closing a third one or more switches to couple the first power line of the second array to a power supply node at the second intermediate voltage level.

11. The method of claim 10, further comprising closing a fourth one or more switches to couple the second power line of the first array to a power supply node at the first intermediate voltage level.

12. The method of claim 10, wherein:

the second intermediate voltage level is greater than the first intermediate voltage level;

a voltage difference between the first intermediate voltage level and the upper reference voltage level is greater than half the voltage difference between the lower reference voltage and the upper reference voltage; and

a voltage difference between the second intermediate voltage level and the lower reference voltage level is greater than half the voltage difference between the lower reference voltage and the upper reference voltage.

13. A circuit configuration for use in recycling bit line charges comprising:

a first set of switches to selectively couple a first power line of a first array of bit line sense amplifiers to a power supply node at an upper reference voltage level and to selectively couple a second power line of a second array of bit line sense amplifiers to a power supply node at a lower reference voltage level;

a second set of switches to selectively couple a second power line of the first array to a power supply node at a first intermediate voltage level and to selectively couple a first power line of the second array to a power supply node at a second intermediate voltage level higher than the first intermediate voltage level;

a third set of switches to selectively precharge the first and second power lines

of the first array to a first precharge voltage level and to selectively precharge the first and second power lines of the second array to a second precharge voltage level; and

a fourth set of one or more switches to selectively couple the second power line of the first array to the first power line of the second array.

14. The circuit configuration of claim 13, wherein the third set of switches comprises at least one switch to selectively couple the first and second power lines of the first array and at least one switch to selectively couple the first and second power lines of the second array.

15. A memory device comprising:

at least first and second arrays of bit line sense amplifiers to sense bit lines of memory cells of the memory device;

a voltage regulator with output nodes for at least an upper voltage reference, first and second intermediate voltages, and a lower voltage reference; and

sensing control circuitry configured to precharge first and second power lines of the first array to a first precharge level, precharge first and second power lines of the second array to a second precharge level, transfer charge from the second power line of the first array to the first line of the second array, couple the second power line of the first array to the first intermediate voltage output node, and couple the first power line of the second array to the second intermediate voltage output node.

16. The memory device of claim 15, wherein the control circuitry is further configured to, subsequent to precharging the first and second lines of the first and second arrays:

couple the first power line of the first array to the upper reference voltage output node; and

couple the second power line of the second array to the lower reference voltage output node.

17. The memory device of claim 15, wherein the controller is configured to precharge the first and second lines of the first array by momentarily coupling the first and second lines of the first array.

18. The memory device of claim 15, wherein the difference between the second intermediate voltage level and the lower reference voltage level is greater than one half the difference between upper reference voltage level and the lower reference voltage level.

19. The memory device of claim 15, wherein the difference between the first intermediate voltage level and the upper reference voltage level is greater than one half the difference between upper reference voltage level and the lower reference voltage level.

20. The memory device of claim 15, wherein the difference between the first intermediate voltage level and the upper reference voltage level is greater than one half the difference between a ground reference and a supply voltage of the memory device.